UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/313,659	05/18/99	YANG W	SEC.636

MM91/0815

JONES AND VOLENTINE LLP
SUITE 150
12200 SUNRISE VALLEY DRIVE
RESTON VA 20191

EXAMINER	
RAO,S	
ART UNIT	**PAPER NUMBER**
2814	4

DATE MAILED: 08/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/313,659	Yang, W-S et al.
Examiner	**Group Art Unit**
S.H. Rao	2814

☒ Responsive to communication(s) filed on *May 18, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-19* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-19* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings incorporating the changes required by the draftsperson and listed on the enclosed PTO-948 will be required when the application is allowed.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The following title is suggested : Method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region.

Claim Rejections - 35 U.S.C. § 112

4. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or

use the invention. Claim 14 recites the interlayer insulating layer as having two etching steps wherein the first etching step is at least five times higher than the second etching rate.

To specification does not disclose the interlayer insulating layer has having two different rates of etching. Therefore the recitation is not supported by the specification. Appropriate correction is required.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1,10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 lines 15 and 16 it is unclear what applicants' mean by "first gate spacers". It is believed that they mean the gate spacers of the third gate, if this is correct than claim 1 has to be amended to reflect the spacers in line 15 and 16 refer to the spacers of the third gate .

Lines 19 and 20 state, " ...adjacent to the first spacers adjacent to the second and third gates". It is unclear what is adjacent to the second and third gates. It is assumed that applicants' are referring to the first spacers of the second and third gates respectively.

Again amendment is needed to clearly specify what applicants desire to covered by their claims.

Similarly line 22-23 second gate and second spacers, lines 24-25 and 27-28 refer to several gates and spacers and their relationship must be clearly established.

Claim 10 line 8 the sixth word "for" is not clear.

Claim 12 line 2 the "," after the tenth word is not clear.

Appropriate correction is required for all the above rejections.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 5,654,213, herein after Choi and further in view of Kashihara et al. U.S. P No. : 5,567,964 (herein after Kashihara).

With respect to claim 1 Choi discloses a method of fabricating MOS transistor with double sidewall spacers in p-well and Single sidewall spacers in the n-well region including the steps of : forming a device isolation region (25 Choi Fig.2), Forming first impurity ions of low concentration in a first portion adjacent the second and third gates using the second and third gates as a mask (See Choi fig. 9) the recitation to form a first impurity diffusion region of a first conductivity type, only states an obvious result and therefore cannot be given any patentable weight.

Forming first gate spacers on lateral sides of the first , second and third gates. (See Choi fig. 10).

implanting second impurity ions of low concentration into a second portion of the semiconductor substrate adjacent to the first gates and spacers, using the gate and spacers as a mask to form a second impurity diffusion region of a first conductivity type (See Choi fig. 10).

implanting third impurity ions of low concentration into a third portion of the semiconductor substrate adjacent to the third gates and spacers, using the third gate and spacers as a mask to form a third impurity diffusion region of a second conductivity type (See Choi figs. 11 and 12). (additionally it is obvious to repeat the steps of implanting using the first gate and spacers as a mask, the desired number of times).

Forming an insulating layer (See Choi fig.13 #105) over the substrate, first through third gates and the first gate spacers.

Etching the insulating layer in the peripheral region to form second gate spacers (See Choi figs. 14 and 15). The last part of this sentence, "adjacent to the first spacers adjacent to the second and third gates is unclear and therefore cannot be given patentable weight.

implanting fourth impurity ions of low concentration into a fourth portion of the semiconductor substrate adjacent to the second gates and spacers, using the second gate and spacers as a mask to form a fourth impurity diffusion region of a first conductivity type (See Choi figs. 16). (additionally it is obvious to repeat the steps of implanting using the first gate and spacers as a mask several times as desired).

implanting fifth impurity ions of low concentration into a fifth portion of the semiconductor substrate adjacent to the third gates and second spacers, using the third gate and first and second spacers as a mask to form a fifth impurity diffusion region of a second conductivity type (See Choi figs. 17). (additionally it is obvious to repeat the steps of implanting using the first gate and spacers as a mask several times as desired).

Choi does not specifically disclose the formation of a third gate in the peripheral region.

However, Kashihara in fig.1, describes the formation of a third gate in the peripheral region, to control the other devices of that transistor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use additional gates described by Kashihara in Choi's devices to control the other devices of that transistor.

With respect to claim 2 Choi in addition to the teachings stated under claim 1 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

wherein the first conductivity type is n-type. (See Choi fig. 1).

With respect to claim 3 Choi in addition to the teachings stated under claims 1-2 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

wherein the first impurity ions diffused has a lower ion diffusivity than the second impurity ions. (See Choi Col. 2 line 26 first impurity ions is Arsenic and Col.2 line 47 second impurity ions is Boron. It is an inherent property of Arsenic and Boron, that Arsenic has lower ion diffusivity than Boron).

With respect to claim 4 Choi in addition to the teachings stated under claims 1-3 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

wherein the first, second and third gates comprise polysilicon. (See Choi Col.3 lines 33).

4. Claims 5, 6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 5,654,213, herein after Choi and further in view of Kashihara et al. U.S. P No. : 5,567,964 (herein after Kashihara), as applied to claims 1-4 above and further in view of Kim (G.B.(U.K.) 2,257,563).

With respect to claim 5 Choi and Kashihara in addition to the teachings stated under claims 1-4 above, disclose a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region. including the steps of : a first ion implantation.

Choi and Kashihara do not specifically teach the first implantation as being carried out at a dose of 5×10^{12} ions/cm^2 and at an energy of 50 keV to better control the implantation.

However, Kim at page 13 lines 1-2 describes a first phosphorus implantation at a dose of 5 x 10^{12} ions/cm^2 and at an energy of 50 keV, (it well known that the same conditions can be used to implant phosphorus or arsenic).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the dosage taught by Kim in Choi and Kashihara's first implantation step to wherein the first ion implantation is done by using arsenic at a dose of 5 x 10^{12} ions/cm^2 and at an energy of 50 keV. (See Kim- page 13 lines 1-2 phosphorus implantation is stated, but it well known that the same conditions can be used to implant phosphorus or arsenic) to better control the implantation of the ions into the substrate.

With respect to claim 6 Choi in addition to the teachings stated under claims 1- 5 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the well known in the art steps of :

wherein the second ion implantation is done by using phosphorus at a dose of 5 x 10^{12} ions/cm^2 and at an energy of 30 keV. (See Kim page 13 lines 1-2).

5. Claims 7,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 5,654,213, herein after Choi and further in view of

Kashihara et al. U.S. P No. : 5,567,964 (herein after Kashihara), as applied to claims 1-4 above and further in view of Mitsui -U.S. 5,296,401 (herein after- Mitsui).

With respect to claims 7,9 Choi in addition to the teachings stated under claims 1- 6 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of : third ion implantation of low concentration.

Choi and Kashihara do not specifically disclose the third implantation at a dosage of 1x 10^{13} ions/cm^2 and at an energy of 20 keV using Boron or BF_3.

However, Mitsui at Col. 8 lines 44-46 teaches a third ion implantation is done by using Boron or BF_3 at a dose of 1 10^{13} ions/cm^2 and at an energy of 20 keV to better control the implantation of the ions into the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Mitsui's implantation dosage in Choi and Kashihara's method to better control the implantation of the ions into the substrate.

6. Claims 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 5,654,213, herein after Choi and further in view of Kashihara et al. U.S. P No. : 5,567,964 (herein after Kashihara), as applied to claims

1-4 above, and Mitsui -U.S. 5,296,401 (herein after- Mitsui), and further in view of Ong (Morden MOS Technology, McGraw- Hill 1986, herein after Ong).

With respect to claim 10 to the extent understood, Choi in addition to the teachings stated under claims 1- 9 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region, including the steps of : forming an interlayer insulating layer over the substrate and first to third gates (See Mitsui Fig. 1 # 10).

Etching a selected portion of the interlayer insulating layer in the cell array region, using the insulating region as an etch stopper and forming a contact opening adjacent to the first gate. (See Mitsui Col. 10 lines 10-12).

Choi, Kashihara and Mitsui do not specifically teach the formation of an silicide layer over the semiconductor substrate and the second and third gates in the peripheral circuit region.

However Ong at pages 145-146 teaches the formation of a silicide layer over the semiconductor substrate and the second and third gates in the peripheral circuit region to protect the substrate and the gates during subsequent processing steps.

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention, to use Ong's teachings of silicidation in Choi, Kashihara and Mitsui's methods

to form a silicide layer over the semiconductor substrate and the second and third gates in the peripheral region to protect the substrate and the gates during subsequent processing steps and so that the effective sheet resistance can be bought down to 1 or 2 ohms per square range.

With respect to claim 11 to the extent understood, Choi in addition to the teachings stated under claims 1- 10 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

forming a transition metal layer over the substrate and the second and third gates and annealing the substrate and the transition material to form the silicide layer. (See Ong pages 145-146).

With respect to claim 14, to the extent understood, Choi in addition to the teachings stated under claims 1- 10 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

wherein the interlayers are etched at diffferent rates (well known in the art).

With respect to claim 12 to the extent understood, Choi in addition to the teachings stated under claims 1- 11 above, discloses a method of fabricating MOS

transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the steps of :

wherein the substrate and transition metal are annealed while the first thru' fifth impurities are diffused. (See Mitsui Col. 10 lines 55-60, also it is well known in the art to use annealing to diffuse implanted impurities).

With respect to claim 13 to the extent understood, Choi in addition to the teachings stated under claims 1- 12 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the well known in the art steps of :

No patentable weight can be given to the recitation here in because the any remaining portion of the insulating layer after etching will act as a barrier layer. (Cl.13)

With respect to claim 15 to the extent understood, Choi in addition to the teachings stated under claims 1- 13 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the well known in the art steps of :

Claim 15 repeats all the steps of claim 1 and adds the additional limitation of annealing and diffusing the impurity diffusion layers to overlap the first diffusion layer with the second diffusion layer. (See Mitsui- figs. 2 h -2 j).

With respect to claims 16-19 to the extent understood, Choi in addition to the teachings stated under claims 1- 15 above, discloses a method of fabricating MOS transistor with double sidewall spacers in peripheral and Single sidewall spacers in the cell region including the well known in the art steps of :

Claim 16 repeats the steps of claim 2, and therefore the teachings stated under claim 2 is incorporated by reference.

Claim 17 repeats the steps of claim 5, and therefore the teachings stated under claim 5 is incorporated by reference.

Claim 18 repeats the steps of claim 7, and therefore the teachings stated under claim 7 is incorporated by reference.

Claim 19 repeats the steps of claim 9, and therefore the teachings stated under claim 9 is incorporated by reference.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The fax number is (703) 308-7722 or -7724.The Examiner can be normally reached on Monday-Friday from 9.30 a.m. to 6.00 p.m. (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor Ex. Olik Chaudhuri, can be reached at (703) 306-2794.

8. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission at the above mentioned fax numbers.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology center 2800 receptionist at (703) 308-0956.

August 9, 2000.

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800